EUROPEAN UNIVERSITY OF LEFKE

Electrical and Electronics Engineering, Faculty of Engineering

SYLLABUS

2020-2021 Spring Semester

Course Code	Course Name	Course Type	Weekly Course Hours T	A	L	Credits	ECTS	Weekly Time Schedule
COMP228	Digital System Design	Major	3	0	2	4	6	Friday 15:00-17:50 - ONLINE > **Labs to be scheduled!**
Prerequisite		**Prerequisite to**						

Course Lecturer	Soydan Redif	**Office Hours Schedule**	
E-mail		**Office / Room No**	
Phone		**Phone**	
Teaching Assistant	Ahmet Yasli	**Office / Room No**	
E-mail	ayasli@eul.edu.tr		

Catalogue Descriptions	Review of Boolean algebra, truth tables, K-maps, combinational logic; Synchronous sequential circuits; Flip-flops; Counters and shift registers; Sequential logic design; Memory and programmable logic; Registers and counters - design/analysis of counters; Micro operations: arithmetic, logic and shift operation; Parallel register transfer and algorithmic state machines.
Course Objectives	To give students the necessary skills and knowledge in order to: (i) analyse and design of digital clocked sequential circuits; (ii) understand micro operations, parallel register transfer and algorithmic state mahines.
Learning Outcomes	On successful completion of the course, students should be able to understand: (1) Boolean functions and their minimisation, (2) the design combinational and clocked sequential logic circuits, (3) parallel register transfer and algorithmic state machines, (4) the implementation and testing of sequential logic systems,
Textbooks	1 M. Morris Mano, Digital Design, 5th Ed, Prentice Hall, 2012. ISBN-10: 0-13-277420
	2 J. F. Wakerly, Digital Design: Principles and Practices, 4th Ed, Prentice Hall, 2019. ISBN-10: 013446009X

WEEK	Date	TOPICS	Reference No - Section
Week 1	01-05/03/21	Review of number systems and Boolean algebra	1: 1.1-1.8
Week 2	08-12/03/21	Review of logic gates and gate-level minimisation	1: 2.1-2.4
Week 3	15-19/03/21	Combinational circuits: analysis and design procedures	1: 2.5-2.9
Week 4	22-26/03/21	Sequential logic - analysis of sequential logic circuits	1: 3.1-3.4
Week 5	29-02/03-04/21	Analysis of exemplar clocked sequential circuits	1: 3.3; 3.5-3.7
Week 6	05-09/03/21	Additional exercises on analysis of clocked sequential circuits	1: 4.1-4.4;4.6
Week 7	10-18/04/21	**Midterm Exam**	-
Week 8	19-23/04/21	Design of clocked sequential logic	1: 5.1-5.4
Week 9	26-30/04/21	Additonal exercises on design of clocked sequential logic	1: 5.2; 5.5-5.6; 5.9
Week 10	03-07/05/21	Registers and counters - design/analysis of counters	1: 5.2; 5.5-5.6; 5.9
Week 11	10-14/05/21	Memory: RAM, ROM, PLD, PAL, memory decoding	1: 6.4-6.6
Week 12	17-21/05/21	Micro operations: arithmetic, logic and shift operation	1: 7.1-7.3
Week 13	24-28/05/21	Parallel register transfer	1: 7.3; 7.6-7.8
Week 14	31-04/05-06/21	Algorithmic state machines	1: 7.3; 7.6-7.8
Week 15	07-11/06/21	Review material	1: 7.3; 7.6-7.8
Week 16	12-21/06/21	**Final Exam**	-

Evaluation Tools

Evaluation Tool	Quantity	Date	Weight in Total (%)	Weight in Semester Evaluation (%)
Final Exam	1	12-21/06/21	50	
Semester Evaluation			50	
Midterm(s)	1	10-18/04/21	30	60.0
Quiz(zes)				
Project(s)				
Homework(s)				
Laboratory works	5		20	40.0
Attendance				

*** *Lifelong Learning Programme (LLP)* *** Language of Instruction: English