EUROPEAN UNIVERSITY OF LEFKE

Electrical and Electronics Engineering, Faculty of Engineering

SYLLABUS

2019-2020 Spring Semester

Course Code	Course Name	Course Type	Weekly Course Hours			Credits	ECTS	Weekly Time Schedule
			T	A	L			
COMP228	Digital System Design	Major	3	0	2	4	6	Thurssday 09:00-11:50 - AS111 > Labs to be scheduled!
Prerequisite		Prerequisite to						

Course Lecturer	Soydan Redif	Office Hours Schedule	On instructor's timetable.
E-mail			
Phone		Office / Room No	AS-314
Teaching Assistant	Ahmet Yasli	Phone	
E-mail	ayasli@eul.edu.tr	Office / Room No	

Catalogue Descriptions	Review of Boolean algebra, truth tables, K-maps, combinational logic; Synchronous sequential circuits; Flip-flops; Counters and shift registers; Sequential logic design; Memory and programmable logic; Registers and counters - design/analysis of counters; Micro operations: arithmetic, logic and shift operation; Parallel register transfer and algorithmic state machines.
Course Objectives	To give students the necessary skills and knowledge in order to: (i) analyse and design of digital clocked sequential circuits; (ii) understand micro operations, parallel register transfer and algorithmic state mahines.
Learning Outcomes	On successful completion of the course, students should be able to understand: (1) Boolean functions and their minimisation, (2) the design combinational and clocked sequential logic circuits, (3) parallel register transfer and algorithmic state machines, (4) the implementation and testing of sequential logic systems,
Textbooks	1 M. Morris Mano, Digital Design, 5th Ed, Prentice Hall, 2012. ISBN-10: 0-13-277420 2 J. F. Wakerly, Digital Design: Principles and Practices, 4th Ed, Prentice Hall, 2019. ISBN-10: 013446009X

WEEK	Date	TOPICS	Reference No - Section
Week 1	18/02/2020	Review of number systems and Boolean algebra	1: 1.1-1.8
Week 2	25/02/2020	Review of logic gates and gate-level minimisation	1: 2.1-2.4
Week 3	03/03/2020	Combinational circuits: analysis and design procedures	1: 2.5-2.9
Week 4	10/03/2020	Sequential logic - analysis of sequential logic circuits	1: 3.1-3.4
Week 5	17/03/2020	Analysis of exemplar clocked sequential circuits	1: 3.3; 3.5-3.7
Week 6	24/03/2020	Additional exercises on analysis of clocked sequential circuits	1: 4.1-4.4;4.6
Week 7	31/03/2020	Design of clocked sequential logic	1: 5.1-5.4
Week 8	07/04/2020	Additonal exercises on design of clocked sequential logic	1: 5.2; 5.5-5.6; 5.9
Week 9	11-18/04/2020	**Midterm Week**	-
Week 10	21/04/2020	Registers and counters - design/analysis of counters	1: 5.2; 5.5-5.6; 5.9
Week 11	28/04/2020	Memory: RAM, ROM, PLD, PAL, memory decoding	1: 6.4-6.6
Week 12	05/05/2020	Micro operations: arithmetic, logic and shift operation	1: 7.1-7.3
Week 13	12/05/2020	Parallel register transfer and algorithmic state machines	1: 7.3; 7.6-7.8
Week 14	19/05/2020	REVIEW	1: 7.3; 7.6-7.8
Week 15	28-07/05-06/2020	**Final Exam Week**	-